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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/816,933	03/23/2001	Christian Siemers	GR 98 P 8110 P	6157

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EXAMINER	
SIDDIQI, MOHAMMAD A	
ART UNIT	**PAPER NUMBER**
2126	

DATE MAILED: 10/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/816,933	SIEMERS, CHRISTIAN	
	Examiner	Art Unit	
	Mohammad A Siddiqi	2126	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *39-76* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03/23/01* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *19843637.8* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-76 are presented for examination.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

Group I. Claims 1-38 drawn to Microprocessor or multichip or multimodule processor having sequential program control, classified in Class 712, subclass 1.

Group II. Claims 39-76, drawn to Interrupt Processing, classified in Class 710, subclass 260.

3. The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility in a System lacking the interrupt processing, particulars. See MPEP § 806.05(d). also the restriction requirement is based on the interpretation that every dependent claim is dependent on the preceding independent claim (note Applicant's claim numbering).

4. Because the inventions are distinct for the reason given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated proper.

5. A telephone call was made to Greg Mayback on 10/01/2003 to request an oral election to the restriction requirement, and oral election being made for the group of claims 1- 38 with traverse on 10/03/2003 to prosecute the invention of Group I, claims 1-38. Affirmation of this election must be made by applicant in responding to this Office action. Claims 39-76 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

6. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a petition under 37 CFR 1.48(b) and by the fee required under 37 C.F.R. 1.17(h).

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

8. Claims 1-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Kau et al. (6421754) (hereinafter Kau).

9. As per claims 1 and 20, Kau discloses a program-controlled unit (see abstract), comprising: an intelligent core configured (figure 9, element 702,701) to process instructions to be executed (figure 19, col 123, lines 29-67);

a plurality of units selected from the group consisting of internal peripheral units disposed inside the program-controlled unit (figure 9, element 718,702,726), external peripheral units exterior to the program-controlled unit (figure 3, element IN6, and IN7, col 9, lines 1-64), and one or more memory devices (figure 3, element 74, IN6, and IN7, col 9, lines 1-64);

a structurable hardware unit (figure 3, col 9, lines 1-64) selectively forming an application-specifically (figure 45, element 4350, col 49, lines 28-47)

configurable intelligent interface for respectively connecting said intelligent core (figure 9, element 702) and said units (figure 9, col 49, lines 28-47), including an interface connection between said intelligent core and said internal peripheral units (figure 3, col 61, lines1-11), between said intelligent core and said external peripheral units(figure 67,col 61, lines 15-26), , between said intelligent core and said memory devices(figure 3, element 702, 718), and between said plurality of units(figure 9); and

wherein said structurable hardware unit (figure 3) is configured to evaluate and process data (figure 9) and/or signals (col 63, lines66-67) received thereby (fig 9, Col 64, lines 1-8).

10. As per claims 2 and 21, Kau discloses the structurable hardware (figure 3) unit is disposed in circuit (col 2, lines 14-42) terms between said intelligent core (figure 9, element 702) and said plurality of units (col 2, lines 14-42).

11. As per claims 3 and 22, Kau discloses the structurable hardware unit (figure 3) is connected to a multiplicity of potential data (figure 61, element 302, lines 14-36) and signal sources and data and signal destinations (col 48, lines 51-53), and wherein a plurality of multiplexers (figure 61, element

6110, 6120, col 60, lines 14-36) are connected to said structurable hardware unit (figure 3) for selecting current data and signal sources and current data and signal destinations (figure 61, element 6110, 6120, col 60, lines 14-36).

12. As per claims 4 and 23, Kau discloses the data and signal sources (col 48, lines 37-53) and the data and signal destinations comprise (col 48, lines 51-53) units selected from the group of units consisting of said intelligent core (figure 9, element 702), said peripheral units (figure 3), said memory devices (figure 3, element 74, IN6, and IN7, col 9, lines 1-64), and portions of said structurable hardware unit (figure 3, element 74, IN6, and IN7, col 9, lines 1-64).

13. As per claims 5 and 24, Kau discloses a structuring of said structurable hardware (figure 3) unit selectively results in an alteration of given data paths and in a configuration of logic elements (col 43, lines 19-27).

14. As per claims 6 and 25, Kau discloses a structurable hardware unit (figure 3) comprises a clock generation unit generating a clock signal (figure 27, element 2510, col 37, lines 52-57) and a logic block unit connected to receive the clock signal (figure 27, col 34, lines 52-67), said logic block unit

enabling devices to be connected via said structurable hardware unit to cooperate as desired (col 35, lines 1-46).

15. As per claims 7 and 26, Kau discloses the clock generation unit and said logic block unit each contain configurable elements (figure 27, element 2510, col 37, lines 52-67).

16. As per claims 8 and 27, Kau discloses the clock generation unit is formed at least in part by a device selected from the group consisting of a DNF logic configuration (col 35, lines 55), a NAND array (col 32, lines 112), a multiplexer-based logic variant (figure 61, element 6110, 6120, col 60, lines 14-36), and a structurable logic configuration (col 89, lines 47-54).

17. As per claims 9 and 28, Kau discloses the logic block unit is formed at least in part by a device selected from the group consisting of a DNF logic configuration, a NAND array (figure 27, col 35, lines 62-67 and col 36, lines 1-50), a multiplexer-based logic variant, and a structurable logic configuration (figure 61, element 6110, 6120, col 60, lines 14-36).

18. As per claims 10 and 29, Kau discloses the logic block unit comprises at least one logic block subdivided at least partly into individually configurable sub-blocks with predetermined tasks (col 123, lines 1-67).

19. As per claims 11 and 30, Kau discloses one of sub-blocks is configured as a processing device enabled for one of arithmetic and logical processing of data input to said sub-block (col 67 and 68, table).

20. As per claims 12 and 31, Kau discloses one of sub-blocks is configured as a state machine for central sequence control (figure 22, element 2030, lines 15 –42).

21. As per claims 13 and 32, Kau discloses one of sub-blocks is configured as an address calculation device for calculating source and destination addresses (col 67,68, 69,and 70).

22. As per claims 14 and 33, Kau discloses one of sub-blocks is configured as an instruction injection device for injecting instructions into an instruction pipeline of said intelligent core (col 66, lines 55-60).

23. As per claims 15 and 34, Kau discloses the structurable hardware unit (figure 3) is configurable with devices selected from the group consisting of fuses and anti-fuses (col 14, lines 58-67).

24. As per claims 16 and 35, Kau discloses the structurable hardware unit (figure 3) is reversibly configurable (col 143, lines 14-19).

25. As per claims 17 and 36, Kau discloses the structurable hardware unit is configurable based on data representing a desired configuration, and the data are stored in memory devices insertible into a memory or I/O area which is addressible by said intelligent core (figure 57, col 182, lines 57-65).

26. As per claims 18 and 37, Kau discloses a configuration of structurable hardware unit (figure 3) is enabled only at predetermined times (col 151, lines 1-5).

27. As per claims 19 and 38, Kau discloses the program-controlled configuration of structurable hardware unit (figure 3) is enabled at any time (col 128, lines 39-41).

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

U.S. Patent 6598148 to Moore et al.

U.S. Patent 6134707 to Herrmann et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohammad A Siddiqi whose telephone number is (703) 305-0353. The examiner can normally be reached on Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John A Follansbee can be reached on (703) 305-8498. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

MAS

JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100